HM62A16256CBPI Series

Wide Temperature Range Version
4 M SRAM (256-kword × 16-bit)

HITACHI

ADE-203-1102 (Z)
Preliminary
Rev. 0.0
Sep. 8, 1999

Description

The Hitachi HM62A16256CBPI Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62A16256CBPI Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48 bumps chip size package with 0.75 mm bump pitch for high density surface mounting. HM62A16256CBPI is suitable for the application of the mobile phone to reduce both the mount space and weight.

Features

- Single 1.8 V supply: 1.65 V to 2.0 V
- Fast access time: 70 ns (max)
- Power dissipation:
  - Active: TBD (typ)
  - Standby: 0.9 µW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range: –40 to +85°C

Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

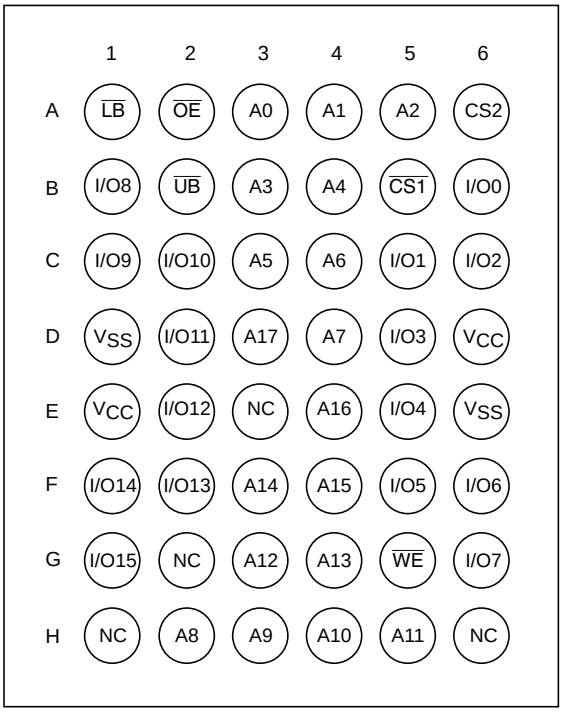
Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HM62A16256CLBPI-7	70 ns	48-bumps CSP with 0.75 mm bump pitch (TBD)
HM62A16256CLBPI-7SL	70 ns	

Pin Arrangement

48-bumps CSP

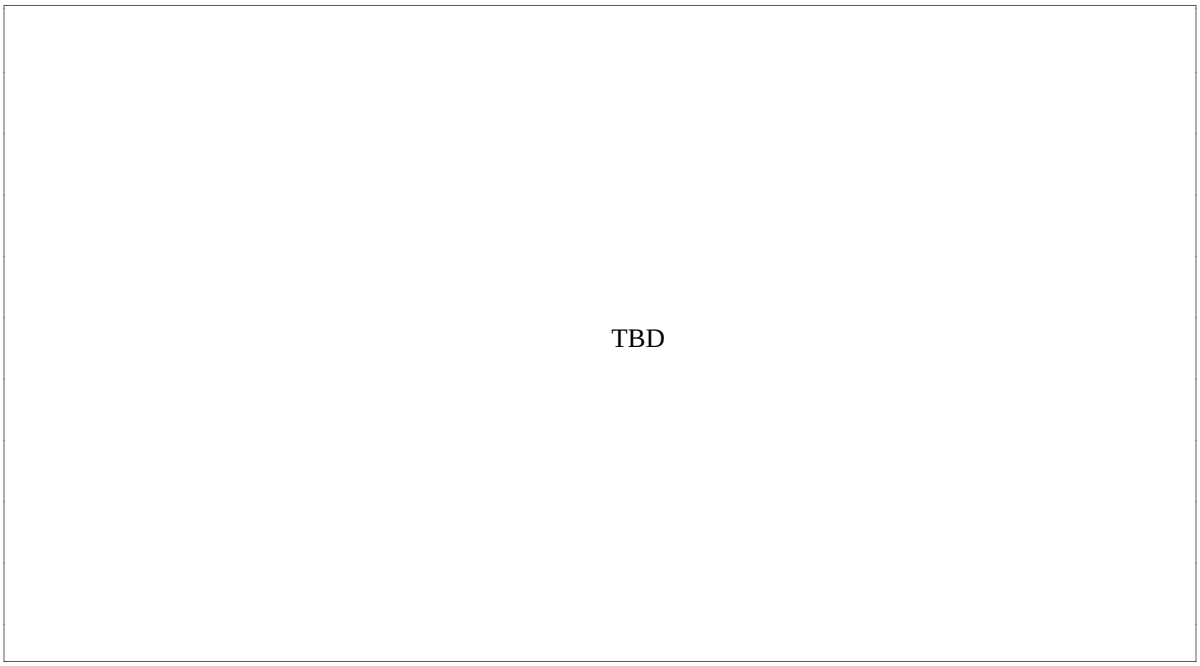


(Top view)

Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.3 to + 2.5	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.3*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–40 to +85	°C

Notes: 1. V_T min: –1.0 V for pulse half-width ≤ 20 ns.
2. Maximum voltage is +2.5 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	1.65	1.8	2.0	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	1.4	—	V_{CC} + 0.2	V	
Input low voltage	V_{IL}	–0.2	—	0.4	V	1
Ambient temperature range	Ta	–40	—	85	°C	

Note: 1. V_{IL} min: –1.0 V for pulse half-width ≤ 20 ns.

DC Characteristics

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, or $\overline{LB}$ = $\overline{UB}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating current	I_{CC}	—	—	2	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	25	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	—	3	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current	I_{SB}	—	—	0.3	mA	CS2 = V_{IL}
Standby current	I_{SB1}*[2]	—	0.5	5	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V
	I_{SB1}*[3]	—	0.5	2	µA	
Output high voltage	V_{OH}	V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA
Output low voltage	V_{OL}	—	—	0.2	V	I_{OL} = 100 µA

Notes: 1. Typical values are at V_{CC} = 1.8 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L-version.
3. This characteristic is guaranteed only for L-SL version.

Capacitance (Ta = +25°C, f = 1.0 MHz)

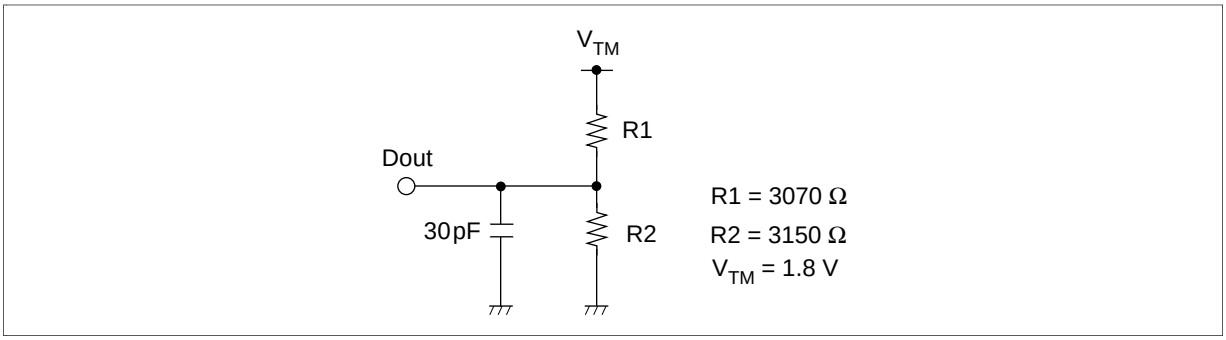
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 1.65 V to 2.0 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.2 V, V_{IH} = V_{CC} – 0.2 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 0.9 V
- Output load: See figure (Including scope and jig)



Read Cycle

		HM62A16256CBPI			
		-7			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	70	—	ns	
Address access time	t_{AA}	—	70	ns	
Chip select access time	t_{ACS1}	—	70	ns	
	t_{ACS2}	—	70	ns	
Output enable to output valid	t_{OE}	—	40	ns	
Output hold from address change	t_{OH}	10	—	ns	
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	—	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	2, 3
	t_{CLZ2}	10	—	ns	2, 3
$\overline{LB}$, $\overline{UB}$ enable to low-z	t_{BLZ}	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	25	ns	1, 2, 3
	t_{CHZ2}	0	25	ns	1, 2, 3
$\overline{LB}$, $\overline{UB}$ disable to high-Z	t_{BHZ}	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	ns	1, 2, 3

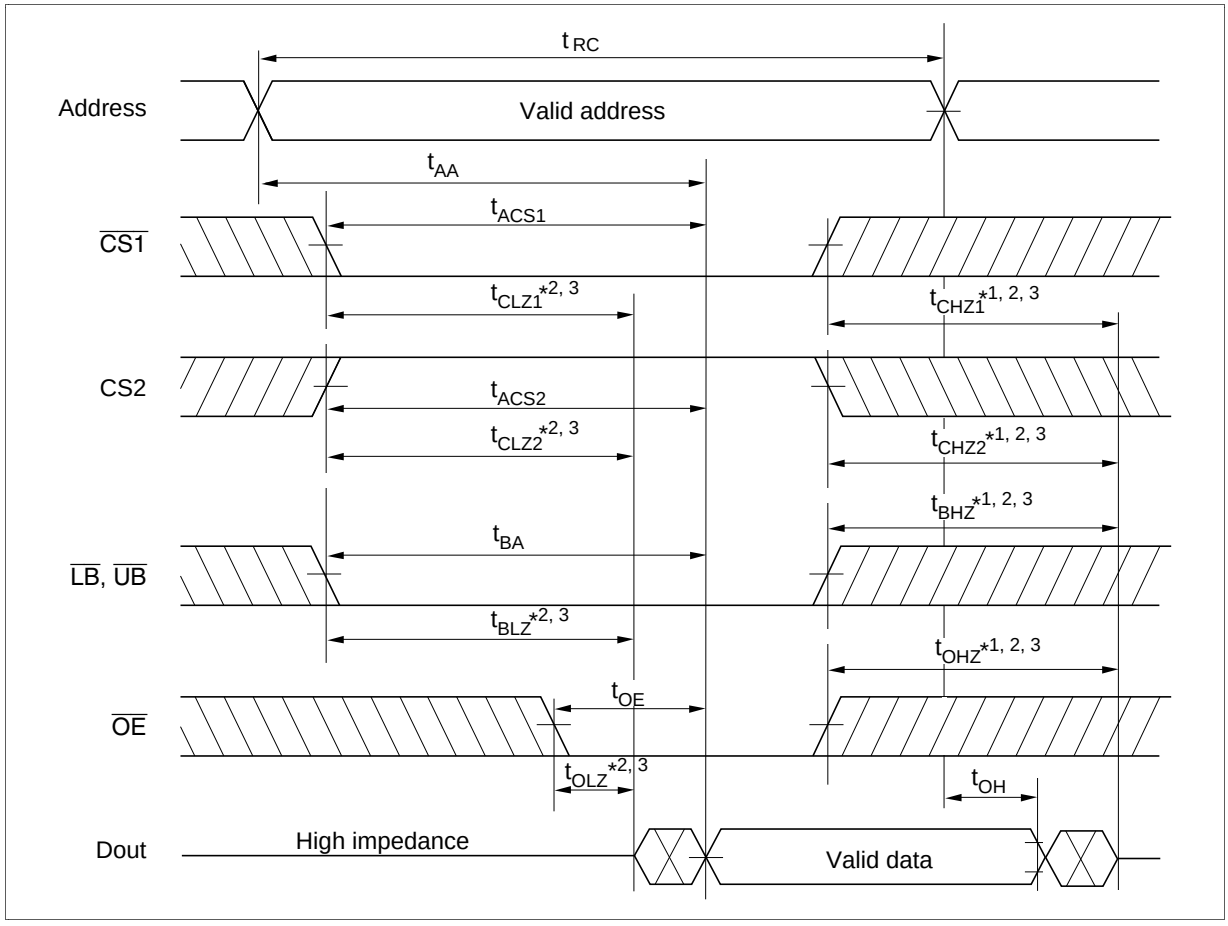
Write Cycle

		HM62A16256CBPI			
		-7			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	70	—	ns	
Address valid to end of write	t_{AW}	60	—	ns	
Chip selection to end of write	t_{CW}	60	—	ns	5
Write pulse width	t_{WP}	50	—	ns	4
$\overline{LB}$, $\overline{UB}$ valid to end of write	t_{BW}	55	—	ns	
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	30	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	25	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	25	ns	1, 2

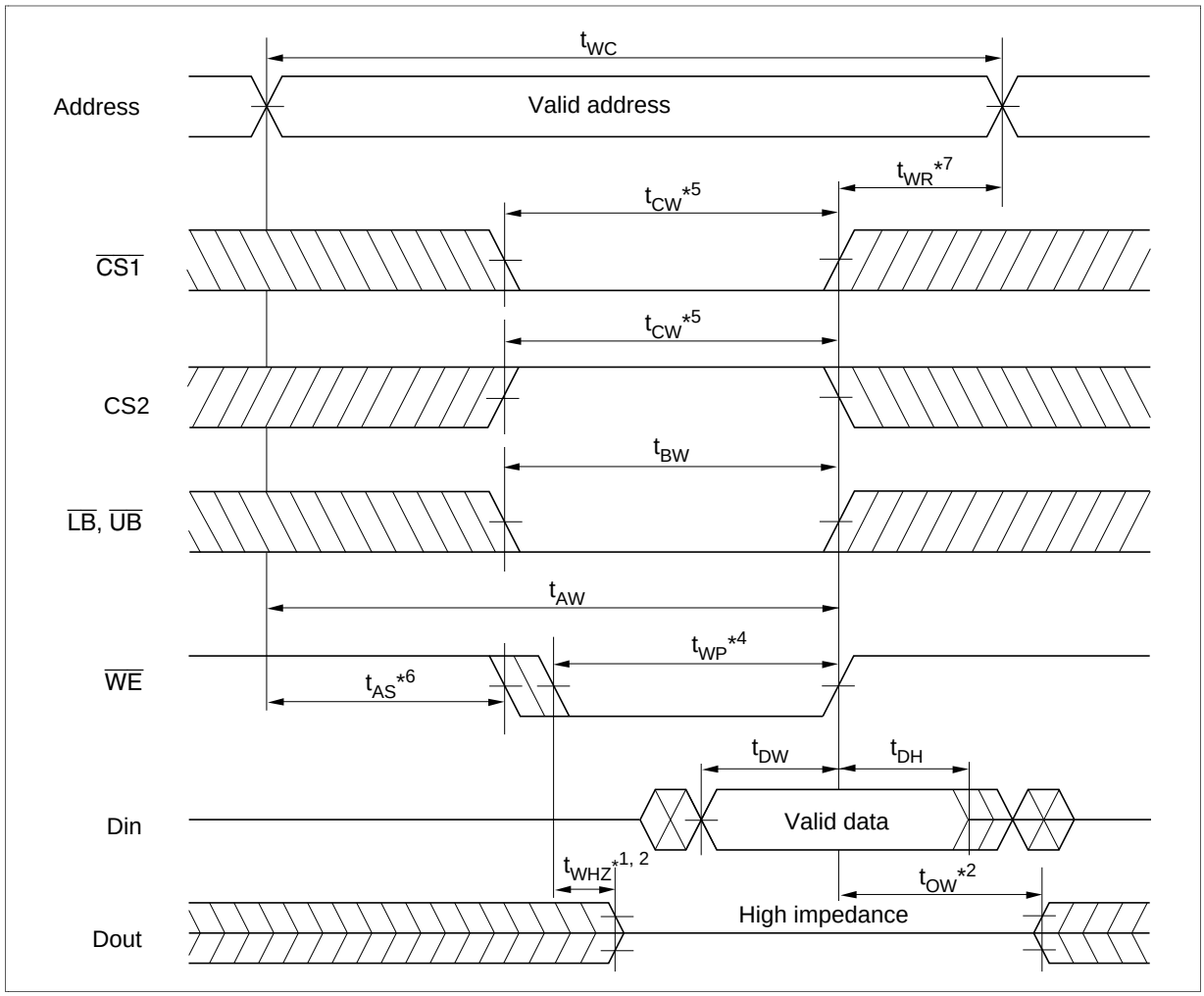
Notes:
1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, a low $\overline{WE}$ and a low $\overline{LB}$ or a low $\overline{UB}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, $\overline{WE}$ going low and $\overline{LB}$ going low or $\overline{UB}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, $\overline{WE}$ going high and $\overline{LB}$ going high or $\overline{UB}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

Timing Waveform

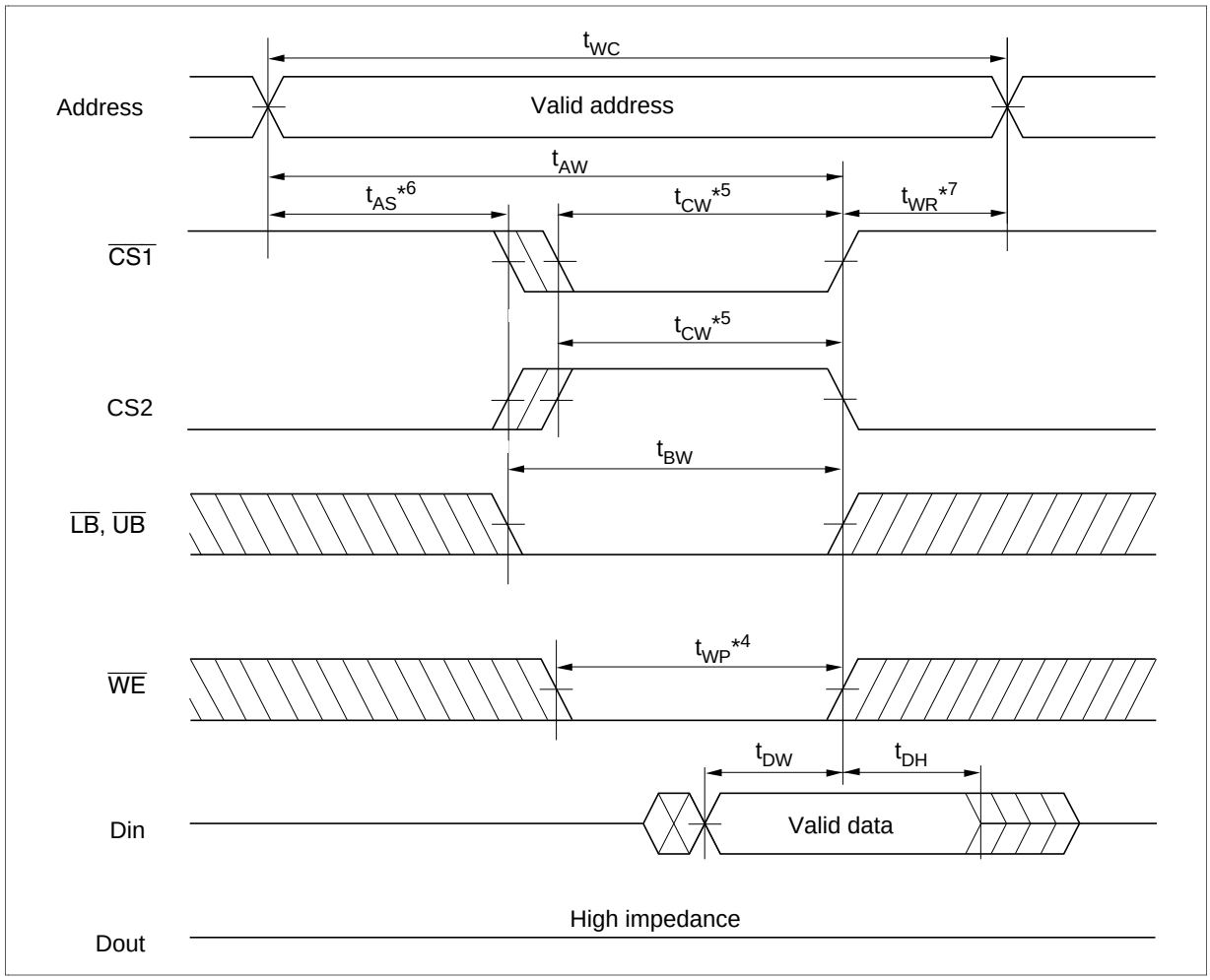
Read Cycle



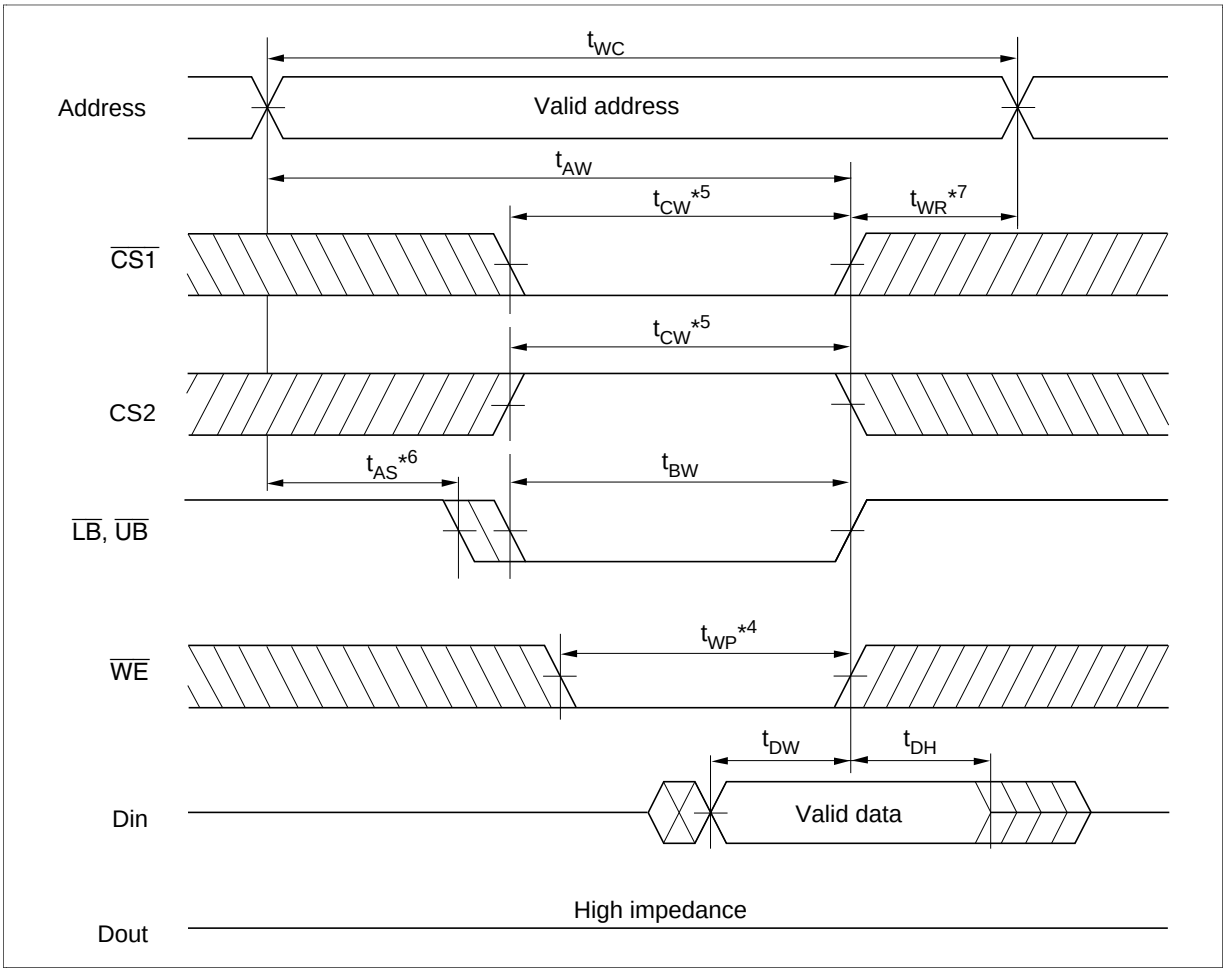
Write Cycle (1) ($\overline{WE}$ Clock)



Write Cycle (2) ($\overline{CS}$ Clock, $\overline{OE}$ = V_{IH})



Write Cycle (3) ($\overline{LB}$, $\overline{UB}$ Clock, $\overline{OE}$ = V_{IH})

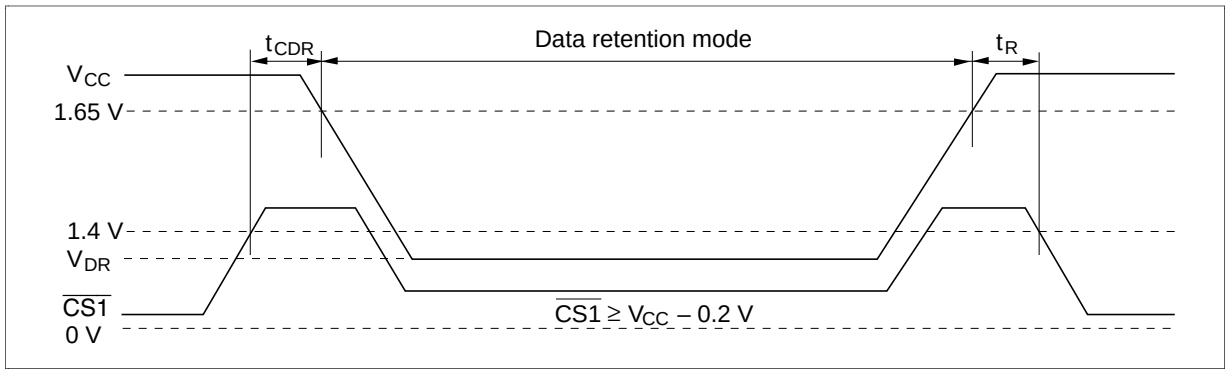


Low V_{CC} Data Retention Characteristics (Ta = –40 to +85°C)

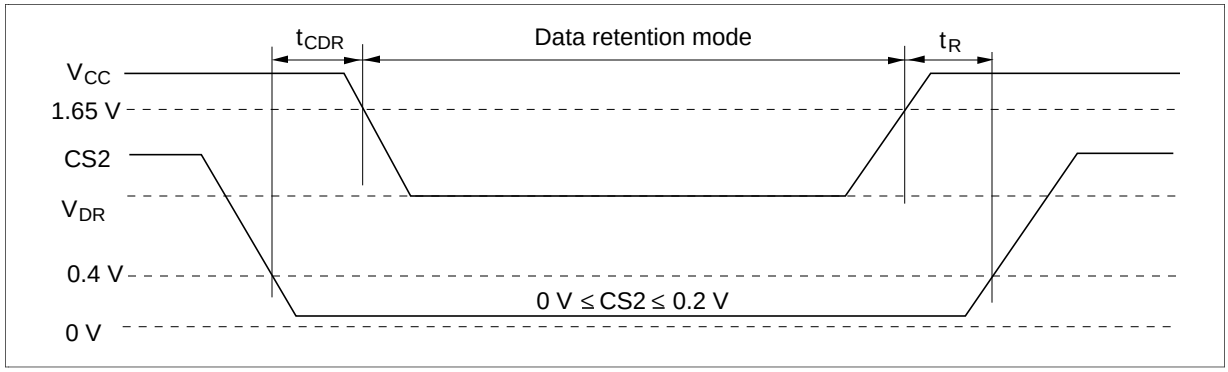
Parameter	Symbol	Min	Typ*4	Max	Unit	Test conditions*3
V_{CC} for data retention	V_{DR}	1.0	—	2.0	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≥ V_{CC} – 0.2 V or (3) $\overline{LB}$ = $\overline{UB}$ ≥ V_{CC} – 0.2 V CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≤ 0.2 V
Data retention current	I_{CCDR}*1	—	0.3	3	µA	V_{CC} = 1.2 V, Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V or (3) $\overline{LB}$ = $\overline{UB}$ ≥ V_{CC} – 0.2 V CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≤ 0.2 V
	I_{CCDR}*2	—	0.3	2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*5	—	—	ns	

Notes: 1. This characteristic is guaranteed only for L-version.
2. This characteristic is guaranteed only for L-SL version.
3. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, $\overline{LB}$, $\overline{UB}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, $\overline{LB}$, $\overline{UB}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$, I/O) can be in the high impedance state.
4. Typical values are at V_{CC} = 1.2 V, Ta = +25˚C and not guaranteed.
5. t_{RC} = read cycle time.

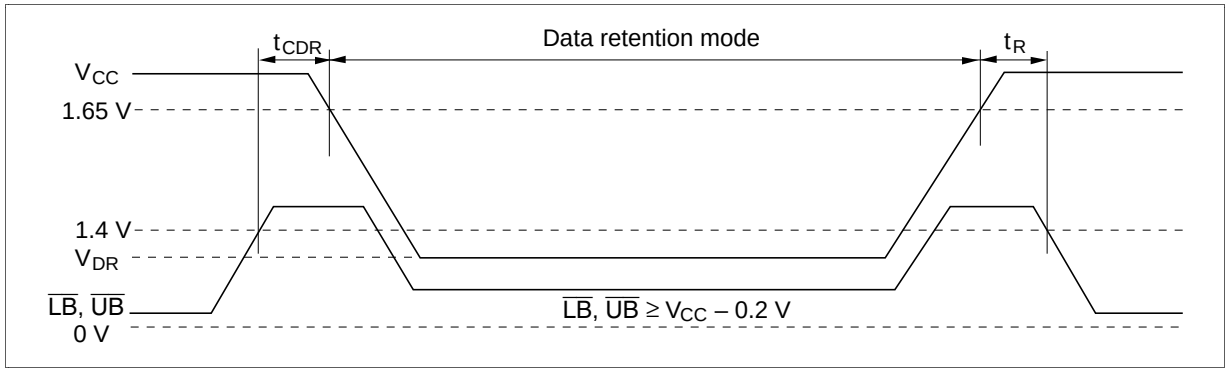
Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



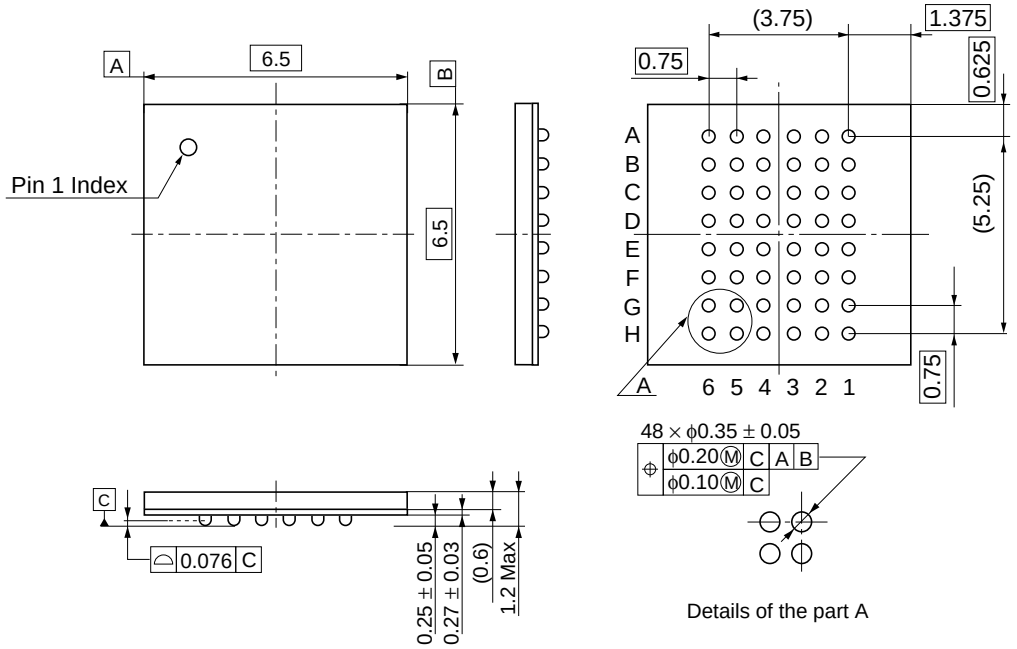
Low V_{CC} Data Retention Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Package Dimensions

HM62A16256CLBPI Series (TBD)

Unit: mm



Details of the part A

Hitachi Code	TBD
JEDEC	—
EIAJ	—
Weight (reference value)	TBD

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Revision Record

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0.0	Sep. 8, 1999	Initial issue		